Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 0325.00063	SERIAL NO. 08/707,694
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	APPLICANT: Rangasayee et al.	
	FILING DATE September 4, 1996	GROUP 2787

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Date	Name	Class	Sub-Class	Filing Date
DMB	4 2 2 9 6 9 9	10/21/80	Frissell	328	63	
DMB	4 4 1 9 6 2 9	12/6/83	O'Brien	328	72	
DMB	4 9 1 8 6 4 1	4/17/90	Jigour et al.	364	716	
DMB	4 9 9 9 5 2 6	3/12/91	Dudley	307	269	
DMB	5 0 4 6 0 3 5	9/3/91	Jigour et al.	364	716	
DMB	5 3 4 1 0 4 4	8/23/94	Ahanin et al.	307	465	
DMB	5 3 8 6 1 5 5	1/31/95	Steele et al.	326	37	
DMB	5 5 1 0 7 4 2	4/23/96	Lemaire	327	146	
DMB	5 5 8 9 7 8 2	12/31/96	Sharpe-Geisler	326	38	
DMB	5 6 5 2 5 3 6	7/29/97	Nookala et al.	327	298	
DMB	5 6 7 0 8 9 6	9/23/97	Diba et al.	326	40	

FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Class	Sub-Class	Transl. Yes	Transl. No

OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent Pages, etc.)

	Nazarian et al., U.S.S.N. 08/626,043, CLOCK DISTRIBUTION ARCHITECTURE AND METHOD FOR HIGH SPEED CPLDS, filed on April 1, 1996.
	Rangasayee, U.S.S.N. 08/699,048, CPLD STRUCTURE WITH IMPROVED SUPPORT FOR CLOCKS, OUTPUT ENABLES AND RESET/PRESET CONDITIONS, filed on August 21, 1996.
	Babar Raza et al., U.S.S.N. 08/587,659, CIRCUIT FOR HIGH SPEED SERIAL PROGRAMMING OF PROGRAMMABLE LOGIC DEVICES, filed on January 17, 1996.

Examiner Dennis M. Butler	Date Considered 1-21-00

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DMB	5 6 8 4 4 3 4	11/4/97	Mann et al.	331	16	

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